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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,842	07/31/2003	Chia-Ta Hsieh	252016-2390	1038

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THOMAS, KAYDEN, HOSTEMEYER & RISLEY LLP
100 GALLERIA PARKWAY
SUITE 1750
ATLANTA, GA 30339

EXAMINER	
NGUYEN, DAO H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/631,842	HSIEH, CHIA-TA	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 07/31/2003 through 04/18/2005, claims 16-59 are active in this application.

Applicant made a provisional election **without traverse** to prosecute the invention of Group II, claims 16-59, drawn to methods of fabricating semiconductor devices. Affirmation of this election was made in the Response to Restriction Requirement, and made of record as Paper No. 0405.

Claim(s) 1-15 have been cancelled.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 10/29/2003. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Specification

3. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim(s) 16-59 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,851,881 to Lin et al., in view of the following remarks.

Regarding claims 16 and 28, Lin discloses a method of fabricating a self-aligned conductive region to active region structure, as shown in figs. 1-3, comprising:

providing a semiconductor region within a substrate 10 extending to a surface,

forming a gate insulator layer 30 (or 41 (over the MONOS gate area 24 and source/trench area 79)) over said semiconductor region 10;

forming, sequentially, a conductive layer 32 (or 44), an insulator layer 41 (or 42) and a hard mask layer 42 (or 43) over said gate insulator layer 30;

patterning said gate insulator layer 30 (or 41), said conductive layer 32 (or 44), said insulator layer 41 (or 42) and said hard mask layer 42 (or 43) to form tiered parallel stripes;

forming a spacer insulator layer 47 over the sidewalls of said parallel stripes;

forming trenches 71 in said semiconductor region 10 between said parallel stripes;

depositing an insulator filler layer 70 so that said trenches 71 and the space between said parallel stripes are filled with said insulator filler layer 70;

planarizing so that said insulator filler layer 70 above top of said insulator layer is removed and said hard mask is removed;

etching said filler layer so that it just fills said trenches (see col. 6, lines 37-41);

removing said insulator layer 30/41 and said insulator spacer layer 47;

patterning said conductive layer to form separated conductive regions, or separated floating gate.

See also col. 4, line 47 to col. 6, line 57.

Lin does not explicitly discuss about an insulator liner layer over sides of the trenches 71, nor about the number of tiered parallel stripes. However, Lin does teach about growing a pad oxide having a thickness of about 300 to 500 Å over the substrate after the trenches 71 being etched (see col. 6, lines 29-32). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the pad oxide layer can form, or modified to form, a liner layer over the sides of the

trenches 71 to prevent ions or electrodes moving back and forth between the semiconductor region and the nitride filled within the trenches 71. In addition, it would have been common and well known in the art that a semiconductor structure can be formed to have multiple active areas in a semiconductor regions, isolated by multiple trench isolations. Such multiple formation involves only routine skills in the art. The number of active areas or tiered parallel stripes in a structure depends on the use of the structure, and it is easy for one of ordinary skills in the art to form a structure with desired number of active areas or tiered parallel stripes once such person can form structures with one or more active areas.

Regarding claims 39 and 50, Lin discloses a method of fabricating a self-aligned conductive region to active region structure, as shown in figs. 1-3, comprising:

providing a semiconductor region within a substrate 10 extending to a surface,

forming a gate insulator layer 30 (or 41, (over the MONOS gate area 24 and source/trench area 79)) over said semiconductor region 10;

forming, sequentially, a conductive layer 32 (or 44) and an insulator layer 41 (or 42 over said gate insulator layer;

patterning said gate insulator layer 30/41, said conductive layer 32/44 and said insulator layer 30/41 to form tiered parallel stripes;

forming a spacer insulator layer 47 over the sidewalls of said parallel stripes;

forming trenches 71 in said semiconductor region 10 between said parallel stripes;

depositing an insulator filler layer 70 so that said trenches and the space between said parallel stripes are filled with said insulator filler layer 70;

planarizing so that said insulator filler layer 70 above top of said insulator layer is removed;

etching said filler layer so that it just fills said trenches;

removing said insulator layer 41/42 and said insulator spacer layer 47;

patterning said conductive layer 32/44 to form separated conductive regions, or to form separated floating gates. See also col. 4, line 47 to col. 6, line 57.

Lin does not explicitly discuss about an insulator liner layer over sides of the trenches 71, nor about the number of tiered parallel stripes. However, Lin does teach about growing a pad oxide having a thickness of about 300 to 500 Å over the substrate after the trenches 71 being etched (see col. 6, lines 29-32). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the pad oxide layer can form, or modified to form, a liner layer over the sides of the trenches 71 to prevent ions or electrodes moving back and forth between the semiconductor region and the nitride filled within the trenches 71. In addition, it would have been common and well known in the art that a semiconductor structure can be formed to have multiple active areas in a semiconductor regions, isolated by multiple trench isolations. Such multiple formation involves only routine skills in the art. The number of active areas or tiered parallel stripes in a structure depends on the use of the structure, and it is easy for one of ordinary skills in the art to form a structure with

desired number of active areas or tiered parallel stripes once such person can form structures with one or more active areas.

Regarding claims 17, 29, 40, and 51, Lin discloses the structure wherein said semiconductor region is a silicon region. See col. 4, lines 58-62.

Regarding claims 18, 30, 41, and 52, Lin discloses the structure wherein said substrate is a silicon substrate. See col. 4., lines 58-62.

Regarding claims 19, 31, 42, and 53, Lin discloses the structure wherein said gate insulator regions are oxide regions. See col. 2, lines 11-25.

Regarding claims 20, 32, 43, and 54, Lin discloses the structure wherein said insulator liner layer is a grown oxide layer. See col. 6, lines 29-31.

Regarding claims 21, 33, 44, and 55, Lin discloses the structure wherein said insulator filler layer is an HDP oxide layer. See col. 6, lines 32-67 and col. 11, lines 13-28.

Regarding claims 22, 34, 45, and 56, Lin discloses the structure wherein said conductive layer is composed of doped polysilicon. Col. 5, lines 1-52.

Regarding claims 23, 35, 46, and 57, Lin discloses the method wherein said insulator layer is a nitride layer. See col. 4, line 49 to col. 6, line 41.

Regarding claims 24, and 36, Lin discloses the method wherein said hard mask layer is an oxide layer. See col. 4, line 49 to col. 6, line 41.

Regarding claims 25, 37, 47, and 58, Lin discloses the method wherein said insulator spacer layer is a nitride layer. See col. 4, line 49 to col. 6, line 41.

Regarding claims 26, 38, 48, and 59, Lin discloses the method wherein said planarizing is performed using CMP. See col. 4, line 49 to col. 6, line 41.

Regarding claims 27, and 49, Lin discloses the structure wherein said conductive regions are gates of semiconductor integrated circuit devices. See col. 6, lines 42-67.

Conclusion

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
April 29, 2005